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EXAMINER

VINH, LAN

ART UNIT

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6

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/902,931	MARTIN, KIRK
	Examiner	Art Unit
	Lan Vinh	1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 11 July 2001.

2a) This action is **FINAL**.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) 22-28 and 34 is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-21 is/are rejected.

7) Claim(s) 29-33 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.

4) Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election of Group I, claims 1-21, 29-33 in Paper No. 5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### ***Claim Objections***

2. Claim 29 is objected to because of the following informalities: In line 5 of claim 29, the term "in the" appears to be a typographical error because the examiner believes that the applicants intend to use the term "therein". The examiner suggests replacing "in the" with --therein-- to clarify the claim language. Appropriate correction is required.

Claims 5, 10, 17, 20, 30 are objected to because of the following informalities: In line 1 of claim 5, 10, 17, 20, 30, the term "the flowing the etchant" appears to be a typographical error, the examiner suggests replacing the term "the flowing the etchant" with --the flowing of the etchant-- to clarify the claim language. Appropriate correction is required.

3. For the purpose of examination, the claim language of "a thickness less than about 0.5 mm" is best understood by the examiner as a thickness less than 0.5 mm. The term "inactive surfaces" are defined in page 5 and fig. 2 of the specification as a back surface of the semiconductor die.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5, 8, 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gigante (US 4,372,803) in view of Ellerson et al (US 5,252,179)

→ Gigante discloses a method for etch thinning silicon device. This method comprises the steps of:

sawing a semiconductor wafer into many individual units or chips 10 (col 2, lines 32-34), which reads on providing a semiconductor die, fig. 1 shows that chip/die 10 having an exposed surface 16 disposed between the first and second edges of the chip/die 10

etching the chip/die 10 with the thinning etchant (col 2, lines 36-37, fig. 2 of Gigante shows that the etchant etches the exposed surface 16 from the first to the second edge to thin the chip/die 10), which reads on etching across the exposed surface from the first edge to the second edge with an etchant to thin the semiconductor die

Unlike the instant claimed invention as per claim 1, Gigante does not specifically disclose flowing an etchant across the exposed surface of the die to thin the semiconductor die.

However, Ellerson discloses a method for selectively etching a encapsulating chip//die comprises the step of flowing an etchant across the surface of a chip/die 11 in

a closed/sealed chamber to remove material from the chip (col 3, lines 50-59 ), which reads on flowing an etchant across the a surface of the die to thin the semiconductor die.

Hence, one skilled in the art would have found it obvious to modify Gigante step of etching the exposed surface of the chip/die using the thinning etchant by flowing an etchant across the a surface of the die to thin the semiconductor die as per Ellerson because Ellerson teaches that by flowing the etchant across the die, the used etchant solution is collected and recycled through the apparatus, thus reducing the amount of etchant solution required (col 2, lines 65-68, col 3, lines 1-5)

Regarding claim 2, Gigante discloses using a thinning etchant mixture of hydrofluoric acid, nitric acid and acetic acid (col 2, lines 41-42)

The limitation of “the flowing the etchant is performed in a sealed chamber” as recited in claim 5 has been discussed above.

Regarding claim 8, since Gigante discloses the step of etching the exposed surface of the chip/die 10 with an acidic solution subsequent after etching the exposed surface with the etchant (col 4, lines 34-38), one skilled in the art would also have found it obvious to modify Gigante step of etching the exposed surface of the chip/die using the acidic solution by flowing an etchant (acidic solution) across the a surface of the die as per Ellerson because Ellerson teaches that by flowing the etchant/acidic solution across the die, the used solution is collected and recycled through the apparatus, thus reducing the amount of etchant/acidic solution required (col 2, lines 65-68, col 3, lines 1-5)

Regarding claim 11, fig. 5-6 of Gigante shows that the mixture of hydrofluoric acid, nitric acid and acetic acid is mixed in a spherical mixing chamber 22.

Regarding claim 12, fig. 2 of Gigante shows that the chip/die 10 having an upper unexposed surface 14 disposed within an encapsulant , the exposed surface 16 is being exposed through a cavity formed in the encapsulant.

6. Claims 3, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gigante (US 4,372,803) in view of Ellerson et al (US 5,252,179) and further in view of Harris et al (US 4,359,360)

Gigante as modified by Ellerson has been described above in paragraph 5. Unlike the instant claimed invention as per claim 3, Gigante and Ellerson do not disclose the specific etchant flow rate across the exposed surface of the chip/die.

However, Harris, in a method for selectively etching a encapsulating semiconductor device, teaches that the etchant flow rate can be controlled to affect the result of the etching step (col 1, lines 67-68, col 2, lines 58-60)

Thus, Harris serves as evidence that the etchant flow rate is a "result effective variable". It has been held that the discovery of an optimum value for the result effective variable is within the purview of routine experimentation by the person of ordinary skill in the art. In re Boesch, 617 F.2d 272, 276, 205 USPQ 215, 219 (CCPA 1980 )

Unlike the instant claimed invention the instant claimed invention as per claim 4, Gigante and Ellerson do not disclose that the flow of the etchant across the exposed surface is turbulent.

Harris also discloses the step of creating turbulent flow of etchant across an encapsulating semiconductor device (see abstract)

Hence, one skilled in the art would have found it obvious to use a turbulent flow of etchant across Gigante and Ellerson exposed chip/die surface to result in complete etching as taught by Harris (col 1, lines 67-68)

7. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gigante (US 4,372,803) in view of Ellerson et al (US 5,252,179) and further in view of Miller (US 5,064,498)

Gigante as modified by Ellerson has been described above in paragraph 5. Regarding claims 6-7, although Gigante and Ellerson disclose the steps of forming an oxide layer on the exposed surface 16 of the chip/die (Gigante col 2, lines 27-28 ) and etching the surface using an acidic solution before/precede the step of thinning the die with the etchant (Gigante, col 2, lines 15-17 ), Gigante and Ellerson do not specifically disclose flowing an acidic solution comprises HF to partially remove oxide on the exposed surface.

However, Miller discloses a method for backside etch for semiconductor device comprises the step of using an acidic solution comprises HF to remove oxide on the exposed surface of the die (col 2, lines 53-55 )

Since Gigante as modified by Ellerson is related to a method of flowing etchant across the exposed surface, one skilled in the art would have found it obvious to modify Gigante and Ellerson by flowing an acidic solution comprises HF to partially remove

oxide on the exposed surface of the die in view of Miller teaching in order to obtain uniform etch across the exposed surface of the die.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gigante (US 4,372,803) in view of Ellerson et al (US 5,252,179) and further in view of Yu (US 6,238,936)

Gigante as modified by Ellerson has been described above in paragraph 5. Regarding claim 9, Gigante discloses the step of etching exposed surface of the die with an acidic solution of HF acid and acetic acid after the step of thinning the chip/die with the etchant. Gigante and Ellerson differ from the claimed invention as per claim 9 by using an acidic solution of HF acid and acetic acid instead of the acidic solution comprises HF acid and nitric acid.

However, Yu, in a method for etching integrated circuit/semiconductor device, teaches using an acidic solution comprises HF acid and nitric acid to etch silicon (col 1, lines 27-28)

Since Gigante as modified by Ellerson is related to a wet etching method of flowing etchant across the exposed surface, one skilled in the art would have found it obvious to modify Gigante and Ellerson by flowing an acidic solution comprises HF acid and nitric acid as per Yu across the exposed surface of the chip/die because Yu teaches that in the case of wet etching of silicon, it is common to use a solution of HF acid and nitric acid (col 1, lines 27-28)

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gigante (US 4,372,803) in view of Ellerson et al (US 5,252,179) and further in view of Muller (US 5,956,142)

Gigante as modified by Ellerson has been described above in paragraph 5.

Although Gigante and Ellerson discloses flowing a layer of etchant across the exposed surface of the die, Gigante and Ellerson do not disclose the specific thickness of the etchant layer as recited in claim 9.

However, Muller, in a wet etching method, discloses that the thickness of the liquid/etchant layer is variable (col 5, lines 13-15 ) and varying liquid etchant layer thickness effects the progress of etching (col 4, lines 22-25 )

Thus, Muller serves as evidence that the liquid etchant layer thickness is a "result effective variable". It has been held that the discovery of an optimum value for the result effective variable is within the purview of routine experimentation by the person of ordinary skill in the art. In re Boesch, 617 F.2d 272, 276, 205 USPQ 215, 219 (CCPA 1980 )

10. Claims 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gigante (US 4,372,803) in view of Ellerson et al (US 5,252,179) and further in view of Muller (US 5,956,142)

Gigante discloses a method for etch thinning silicon device. This method comprises the steps of:

sawing a semiconductor wafer into many individual units or chips 10 (col 2, lines 32-34), which reads on providing a semiconductor die, fig. 1 shows that chip/die 10 having an exposed surface 16/second surface and upper surface 14/first surface

etching the surface 16/second surface using an acidic solution (col 2, lines 26-28 ), which reads on etching across the second surface of the die using an acidic solution

etching the chip/die 10 with the thinning etchant (col 2, lines 36-37, fig. 2 of Gigante shows that the etchant etches the exposed surface 16 from the first to the second edge to thin the chip/die 10), which reads on etching across the second surface from the first edge to the second edge with an etchant to thin the semiconductor die

etching the exposed surface 16/second surface with a acidic solution of HF acid and acetic acid to produce specular and flat surface (col 3, lines 2-12), which reads on etching across the second surface of the semiconductor die with a second acidic solution to at least partially polish the second surface of the semiconductor die

Unlike the instant claimed invention as per claim 13, Gigante does not specifically disclose flowing an etchant/acidic solution across the exposed surface in the etching steps.

However, Ellerson discloses a method for selectively etching a encapsulating chip//die comprises the step of flowing an etchant (acidic solution ) across the surface of a chip/die 11 in a closed/sealed chamber to remove material from the chip (col 3, lines 50-59 ), which reads on flowing an etchant/acidic solution across the a surface of the die

Hence, one skilled in the art would have found it obvious to modify Gigante etching steps of by flowing an etchant across the a surface of the die as per Ellerson because Ellerson teaches that by flowing the etchant across the die, the used etchant solution is collected and recycled through the apparatus, thus reducing the amount of etchant solution required (col 2, lines 65-68, col 3, lines 1-5)

Gigante and Ellerson do not specifically disclose flowing an acidic solution across the second surface to partially remove oxide on the exposed surface.

However, Miller discloses a method for backside etch for semiconductor device comprises the step of using an acidic solution comprises HF to remove oxide on the exposed surface of the die (col 2, lines 53-55 )

Since Gigante as modified by Ellerson is related to a method of flowing etchant across the exposed surface, one skilled in the art would have found it obvious to modify Gigante and Ellerson by flowing an acidic solution to partially remove oxide on the exposed surface of the die in view of Miller teaching in order to obtain uniform etch across the exposed surface of the die.

Regarding claim 14, Gigante discloses using a thinning etchant mixture of hydrofluoric acid, nitric acid and acetic acid (col 2, lines 41-42)

The limitations of claims 15,16 have been discussed above in paragraph 6.

The limitations of claims 17, 18 have been discussed above in paragraph 10.

The limitation of using a second acidic solution comprises HF acid and nitric acid, as recited in claim 19, has been discussed above in paragraph 8.

The limitation of claim 20 has been discussed above in paragraph 9.

Regarding claim 21, fig. 2 of Gigante shows that the chip/die 10 having an upper unexposed surface 14 disposed within an encapsulant , the exposed surface 16 is being exposed through a cavity formed in the encapsulant.

***Allowable Subject Matter***

11. Claims 29-33 would be allowable if rewritten or amended to overcome the objection to the claims set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 29, the prior art of record fails to disclose the step of inserting a first surface of a first member into the cavity to form a channel between the first surface of the first member and the inactive surface of the semiconductor die. The closest prior art of Ellerson et al (US 5,252,179) discloses the step of inserting a surface of movable housing 70/first member into the cavity 23 to form a channel 22 between a surface of the first member and the diaphragm holder 30 on the side of semiconductor die 11 (fig. 3 )

***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302.

The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.



LV  
February 10, 2003